Listing of the Claims:

52. (Currently Amended) A phased array for controlling a radiation pattern comprising:

an extended resonance circuit having an N plurality of ports;

~~an~~ a respective antenna and a corresponding shunt impedance connected to each port;

the extended resonance circuit including a plurality of first tunable series impedances, ~~one of which~~ wherein a respective first tunable series impedance is connected between ~~each~~ adjacent ones of the N plurality of ports, the respective ~~each~~ first tunable series impedance transforming the admittance of one port of the N plurality of ports coupled to the respective first tunable series impedance to the conjugate of the admittance for a serially adjacent second one of the N plurality of ports such that the voltage at each of the ports is the same magnitude across the extended resonance circuit; and

a power source having an impedance matched to the impedance of an endmost port in the array.

53. (Currently Amended) The phased array of claim 52 wherein each of the first plurality of tunable series impedances is a tunable inductor.

54. (Currently Amended)) The phased array of the claim 53 wherein the respective first tunable series impedance between ~~each port~~ adjacent ones of the ports is a tunable transmission line, and the corresponding shunt impedance is a tunable capacitance.

55. (Currently Amended) The phased array of claim 52 wherein ~~each~~ respective ones of the plurality of first ~~(series)~~ series impedances between ~~each port~~ adjacent ones of the ports includes two serially connected quarter-wave transformers with a corresponding tunable capacitor connected in shunt therebetween.

56. (Currently Amended) The phased array of claim 52 further comprising:
a single biased voltage applied to the endmost port in the array.

57. (Previously Presented) The phased array of claim 52, wherein the phase shift between successive ports is equal.

58. (Currently Amended) The phased array of claim 52 wherein each of the first series tunable impedances is a single series tunable impedance.

59. (Previously Presented) The phased array of claim 52 wherein each of the shunt impedances connected to each port is a single tunable admittance.

60. (Currently Amended) The phased array of claim 52 wherein each of the plurality of shunt impedances is identical for each port in the array and each of the plurality of first series tunable impedances is identical for each port in the array.